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Akira Toriumi received the B.S. degree in physics, the M.S. and Ph.D. degrees in applied physics from the University of Tokyo in Japan, 1978, 1980 and 1983, respectively. He joined R&D Center of Toshiba Corporation in 1983. From Aug. 1988 to Feb. 1990, he was with Massachusetts Institute of Technology as a visiting researcher, on leave from Toshiba Corporation. In May 2000, he moved to the University of Tokyo. He had also been a leader of the high-k gate stack group in MIRAI Project in Japan from 2001 to 2007. He is now interested in high-k dielectric materials and carbon electronics as well as small size Si and Ge devices. He is a member of the JSAP, ECS, MRS and IEEE.

Materials Science and Engineering in Metal/High-k Gate Stacks for Much More Moore CMOS

Metal/High-k gate stack technology will be discussed from the viewpoint of materials science to further extend CMOS down scaling, to precisely tune CMOS performance, and to keep CMOS reliability. Higher-k dielectric material engineering for CMOS, the interface dipole formation, and the carrier scattering mechanism will be particularly paid attention to. Furthermore, high-k dielectrics on Ge or III-V will be also discussed. Materials understanding and control should become rather important in addition to the Poisson scaling.

Key word:
high-k, metal gate, higher-k, interface dipole, carrier scattering