

JEFFREY J. WELSER

IBM Almaden Research Center
650 Harry Road
San Jose, CA 95120
(408) 927-1017

2064 University Avenue
San Jose, CA 95128
(408) 507-3799

welser@us.ibm.com

EDUCATION

Stanford University, Stanford, California.

Doctor of Philosophy in Electrical Engineering, December 1994.

Advisors: Professor James F. Gibbons and Dr. Judy L. Hoyt

Dissertation: *Application of Strained-Silicon / Relaxed-Silicon Germanium Heterostructures to Metal-oxide-semiconductor Field-effect Transistors*

MSEE, June 1989; BSEE, June 1988.

Stanford-In-Berlin, West Berlin, Germany. Fall 1986.

EXPERIENCE

8/95 – present **International Business Machines (IBM):**

Director, Nanoelectronics Research Initiative (IBM/SRC)

IBM Almaden Research Center, San Jose, CA (8/06 – present)

IBM Assignee to Semiconductor Research Corporation (SRC), RTP, NC (8/06 – present)

- Directing \$20M university-based research program, funded by industry-government consortia, on new logic nanoelectronic devices to replace CMOS transistors in the 2020 timeframe
- Research being done at three multi-university centers (INDEX / WIN / SWAN) and NSF Nanoscale Science and Engineering Centers, leveraging large investments by state and federal government
- Established first-of-a-kind partnership with NIST for additional funding 9/07

Director, Next Generation Computing Technology Elements

IBM Almaden Research Center, San Jose, CA (12/03 – 7/06)

- Director in strategy group looking at next generation servers, hardware and software
- Included novel memories, cooling, packaging, and integration for flexible, multi-core architectures
- Managed matrixed team building system prototypes around Cell architecture
- Responsible for delivery of technology and chips for next generation systems
- Interface to Power.org and Venture Capital teams for working with start-ups and small companies

Director, High Performance CMOS Technology and BEOL Integration;

Management Committee Executive for Sony-Toshiba-AMD-IBM Development Alliance,

IBM Microelectronics Hopewell Junction, New York

- Director of development organization consisting of 150 engineers responsible for delivering next-generation SOI-based semiconductor technology (5/03 – 12/03)
- Management Committee Leader for Sony-Toshiba-IBM and AMD-IBM development alliances, approximately 200 development engineers from all four companies (3/02 – 12/03)
- Previous position: Senior Manager for SOI Device Design Groups (4/01 – 4/03)
- Main technical interface for IBM and OEM circuit design groups, for custom SOI IC chips

Executive Technical Assistant to John E. Kelly, Sr. Vice President and Group Executive,

IBM Technology Group Somers, New York (4/00 – 3/01)

- Chosen for corporate staff position, as part of executive training for future leaders
- Engaged with Dr. Kelly on CEO level meetings with clients, analysts and government agencies
- Worked on special projects, including internal corporate task forces on technical strategy, and external relations' projects such as the SUNY-Albany 300mm collaboration and the initiation of the SRC MARCO/FCRP centers.

Research Staff Member (95-99); Manager (99-00). Exploratory Silicon Devices & Circuits, IBM T.J. Watson Research Center Yorktown Heights, New York (8/95 – 3/00)

- Designed, fabricated, and characterized novel silicon device structures and studied device physics. Major accomplishments include demonstration of:
 - Vertical transistor for DRAM, currently being incorporated into a DRAM product
 - 1.5 GHz silicon photodiode for Gbit ethernet
 - Quantum dot FLASH memory device
- Managed group researching advanced circuits, devices, and device physics. Sample projects: nanocrystal FLASH devices, low-power DRAM architecture, thin dielectric physics, stochastic doping effects, and 3D circuit integration (joint DARPA program between IBM & Cornell)

1999 – 2002

Columbia University, New York, New York.

Adjunct Professor, Department of Electrical Engineering (while employed at IBM)

- Teaching graduate / undergraduate “Introduction to Semiconductor Devices”

10/90 - 7/95

Solid State Electronics Laboratory, Stanford University, Stanford, California.

Postdoctoral scholar (1/95 - 7/95) / Research Assistant (10/90 - 12/94).

- **Fabricated the world’s first strained-Si NMOS and PMOS devices**
- Researched growth and material characterization of the Si/SiGe materials system, including the growth of heterojunction bipolar transistors and MOSFETs
- Designed and built a computer automation system to control a CVD reactor

6/89 - 9/90

IBM T.J. Watson Research Center, Yorktown Heights, New York.

Pre-doctoral Researcher. Research directed by Dr. Mordehai Heiblum.

- Designed, fabricated, and characterized ballistic transport devices in GaAs-based heterostructures to study electron and hole transport physics

6/88 - 9/88

Sumitomo Electric, Yokohama, Japan.

Advanced Semiconductor Research and Development Laboratory, Student Intern.

- Fabricated and analyzed low-noise GaAs MESFETs for an MMIC

1/87 - 3/87

Hewlett-Packard, Böblingen, Germany.

- Student Intern, technical marketing for digital signal generators

SELECTED PROFESSIONAL ACTIVITY AND HONORS

- Invited panelist for *President Bush’s Council of Advisors on Science & Technology (PCAST)* on “Public / Private Research Partnerships” Aug, 2007
- Testified for *US House Sub-Committee on Science and Technology, Education and Research* on increasing Science & Technology funding and Services Sciences during NSF Re-authorization Hearings, March, 2007
- General Program Chair for the 2004 *IEEE International Electron Devices Meeting*
- General Program Chair for the 2003 *IEEE/TMS Device Research Conference (DRC)*
DRC Board Trustee (2002 – 2006)
- IEEE Electron Device Society Advisory Committee Member (2005 – present)
- Selected for Executive Leadership Training Courses
IBM Global Development Center Program and Global Business Management Program (100 people annually)
UCLA Anderson School of Management LGBT Leadership Training Institute (4 IBM attendees)
- IBM Graduate Fellowship and Solid State Industrial Affiliates’ Award
Fellowship for graduate study at Stanford University
- F.E. Terman Award for Scholastic Achievement in Engineering
Awarded to top 10 students in Stanford School of Engineering graduating class
- Stanford President Donald Kennedy’s Academic Achievement Award
- United States’ Presidential Scholar
Awarded by Pres. Ronald Reagan to 100 students nationwide
- Phi Beta Kappa and Tau Beta Pi

PUBLICATIONS & PATENTS

Over **50 journal publications and conference presentations**, as well as invited talks and interviews in trade journals and popular media, and **21 US patents issued**. Full list attached.

PROFESSIONAL ACTIVITIES

Government Testimony and Panels

Invited panelist for President Bush's Council of Advisors on Science & Technology (PCAST) on "Public / Private Research Partnerships" Aug, 2007

Testified for US House Sub-Committee on Science and Technology, Education and Research on increasing Science & Technology funding and Services Sciences during NSF Re-authorization Hearings, March, 2007

Industrial reviewer NSF NIRT Review Panel #06-595 "Active Nanostructures and Nanosystems" March, 2007

Industrial reviewer NSF NIRT Review Panel #06-585 "Nano-electronic Circuits and Architectures" Feb, 2007

Professional Affiliations:

International Electrical and Electronics Engineers Society (IEEE)

American Physical Society (APS)

Tau Beta Pi National Engineering Honor Society

Phi Beta Kappa

SRC Value Chain Technical Advisory Board (VCTAB) Member 2003 – 2006

Silicon Nanoarchitectures & Beyond SRC/NSF workgroup 2004-2005

Guest Editor for IEEE Transactions on Electron Devices Special Issues

"Non-classical Si CMOS Devices and Technologies: Extending the Roadmap" May, 2006

"Device Technologies and Circuits Techniques for Power Management" Jan, 2008

IEEE International Electron Devices Meeting 1992 – 2004

Session chair: Single Electron Devices 1998

Silicon Nanoscale Devices 1999

Solid State Devices Sub-Committee Member 1998,1999

Solid State Devices Sub-committee Chair 2000

Emerging Technologies Session Organizer and Chair 2001

Technical Program Vice Chair 2002

Technical Program Chair (2003)

General Chair (2004)

IEEE/TMS Device Research Conference 1993 – 2006

Session chair: Si/SiGe FET Performance and Reliability 1996

Novel Silicon Devices & Structures 1998

Session Organizer: Scaled Silicon Technology 1999

RUMP session panelist: Off-Roadmap Vehicles 1996

Molecules as Transistors? 2004

RUMP session organizer: Super-scaled CMOS or Quantum Dots? 1999

Technical Committee Member 1999 – 2001

Technical Program Chair 2002

General Chair 2003

DRC Board Trustee 2002 - 2006

IEEE Professional Society Activities

Electron Device Society's VLSI Circuits and Technology Committee 2001-present

Electron Device Society's Awards Committee 2004-present

Electron Device Society Advisory Committee Member 2005-present

Technology Management Council 2008

ITRS Emerging Research Devices Working Group 2007-present

Journal Reviews:

IEEE Electron Device Letters, IEEE Transactions on Electron Devices, IEEE Transactions on Nanotechnology, APS Applied Physics Letters, and Solid State Electronics.

PATENTS

1. US5559912 Wavelength-selective devices using silicon-on-insulator (9/24/1996)
2. US5874760 4F-square memory cell having vertical floating-gate transistors with self-aligned shallow trench isolation (2/23/1999)
3. US5895273 Silicon sidewall etching (4/20/1999)
4. US5929477 Self-aligned diffused source vertical transistors with stack capacitors in a 4F-square memory cell array (7/27/1999)
5. US5990509 2F-square memory cell for gigabit memory applications (11/23/1999)
6. US5998292 Method for making three dimensional circuit integration (12/7/1999)
7. US6013548 Self-aligned diffused source vertical transistors with deep trench capacitors in a 4F-square memory cell array (1/11/2000)
8. US6033957 4F-square memory cell having vertical floating-gate transistors with self-aligned shallow trench isolation (3/7/2000)
9. US6034389 Self-aligned diffused source vertical transistors with deep trench capacitors in a 4F-square memory cell array (3/7/2000)
10. US6040210 2F-square memory cell for gigabit memory applications (3/21/2000)
11. US6069381 Ferroelectric memory transistor with resistively coupled floating gate(5/30/2000)
12. US6077745 Self-aligned diffused source vertical transistors with stack capacitors in a 4F-square memory cell array (6/20/2000)
13. US6114725 Structure for folded architecture pillar memory cell (9/5/2000)
14. US6137128 Self-isolated and self-aligned 4F-square vertical FET-trench dram cells (10/24/2000)
15. US6204140 Dynamic random access memory (3/20/2001)
16. US6316309 Method of forming self-isolated and self-aligned 4F-square vertical FET-trench DRAM cells (11/13/2001)
17. US6376873 Vertical DRAM cell with robust gate-to-storage node isolation (4/23/2002)
18. US6440801 Structure for folded architecture pillar memory cell (8/27/2002)
19. US6538299 Silicon-on-insulator (SOI) trench photodiode (3/25/2003)
20. US6583462 Vertical DRAM having metallic node conductor (6/24/2003)
21. US6700145 Capacitor with high charge storage capacity (3/2/2004)

JOURNAL PUBLICATIONS & CONFERENCE PRESENTATIONS

1. "The Semiconductor Industry's Nanoelectronics Research Initiative: Motivation and Challenges for Technology and Design," (**Keynote Invited**) J. Welser, presented at *International Conference on Computer-Aided Design*, San Jose, CA, Nov 2007.
2. "The Quest for the Next Information Processing Technology," (**Invited**), J. Welser, G. Bourianoff, V. Zhirnov, R. Cavin, *Journal of Nanoparticle Research*, to be published Oct 2007.
3. "Nanotechnology at SRC," (**Invited**) S. Hillenius, D. Herr, B. Weitzman, and J. Welser, *IEEE Nanotechnology Magazine*, Sep 2007, p. 3-8.
4. "The Semiconductor Industry's Nanoelectronics Research Initiative: Motivation and Challenges," (**Plenary Invited**) J. Welser, presented at *International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication*, Denver, CO, May 2007.

5. "The Semiconductor Industry's Nanoelectronics Research Initiative: Motivation and Challenges," **(Plenary Invited)** J. Welser, presented at *Frontiers of Nanometrology Conference*, National Institute of Standards and Technology (NIST), Gaithersburg, MD, March 2007.
6. "The Nanoelectronics Research Initiative: Motivation and Challenges," **(Invited)** J. Welser, *American Institute of Physics Session, American Vacuum Society International Symposium*, San Francisco, CA, Nov 2006.
7. "Scaling Issues for Strained Materials," **(Invited)** J. Welser, *Advanced CMOS Workshop, International Conference on Simulation of Semiconductor Processes and Devices*, Monterey, CA, Sep 2006.
8. "The Importance of Innovation," **(Keynote Panel Invited)**, J. Welser, *INTEROP Conference & Trade Show*, Las Vegas, NV, May 2006.
9. "The Micro to Nano Addressing Block (MNAB)," K. Gopalakrishnan, R. S. Shenoy, C. T. Rettner, R. S. King, Y. Zhang, B. Kurdi, L. D. Bozano, J.J. Welser, M. B. Rothwell, M. Jurich, M. I. Sanchez, M. Hernandez, P. M. Rice, W. P. Risk and H.K. Wickramasinghe, presented at *International Electron Devices Meeting*, Washington, DC, Dec 2005.
10. "Future Processors: Modular and Flexible," **(Plenary Invited)** C. Johnson and J. Welser, presented at *International Conference on Hardware/Software Codesign and System Synthesis*, New York, Sep 2005.
11. "Enhancing Mobility for High Performance MOSFETs," **(Invited)** J. Welser, presented at *Materials' Research Society Spring Meeting*, San Francisco, CA, Apr 2004 (B7.3).
12. "High performance CMOS devices on SOI for 90 nm technology enhanced by RSD (raised source/drain) and thermal cycle/spacer engineering," H. Park, W. Rausch, H. Utomo, K. Matsumoto, H. Nii, S. Kawanaka, P. Fisher, S.H. Oh, J. Snare, W. Clark, A.C. Mocuta, J. Holt, R. Mo, T. Sato, D. Mocuta, B.H. Lee, O. Dokumaci, P. O'Neil, D. Brown, J. Suenaga, Y. Li, L. Brown, J. Nakos, K. Hathorn, P. Ronsheim, H. Kimura, B. Doris, G. Sudo, K. Scheer, S. Mittl, T. Wagner, T. Umebayashi, M. Tsukamoto, Y. Kohyama, J. Cheek, I. Yang, H. Kuroda, Y. Toyoshima, J. Pellerin, D. Schepis, Y. Li, P. Agnello, and J. Welser, presented at *International Electron Devices Meeting*, Washington, DC, Dec 2003 (*Technical Digest*, p. 27.4.1).
13. "Strained-Si on SOI MOSFETs," **(Invited)** K. Rim and J. Welser, presented at the *Solid State Devices and Materials Conference*, Tokyo, Japan, Sep 2003.
14. "Performance enhancement on sub-70nm strained silicon SOI MOSFETs on ultra-thin thermally mixed strained silicon/SiG3 on insulator (TM-SGOI) substrate with raised S/D," B.H. Lee, A. Mocuta, S. Bedell, H. Chen, D. Sadana, K. Rim, P. O'Neil, R. Mo, K. Chan, C. Cabral, C. Lavoie, D. Mocuta, A. Chakravarti, R.M. Mitchell, J. Mezzapelle, F. Jamin, M. Sendelbach, H. Kermel, M. Gribelyuk, A. Domenicucci, K.A. Jenkins, S. Narasimha, S.H. Ku, M. leong, I.Y. Yang, E. Leobandung, P. Agnello, W. Haensch, and J. Welser, presented at *International Electron Devices Meeting*, San Francisco, CA, Dec 2002 (*Technical Digest*, p. 946).
15. "A High Performance 90nm SOI Technology with 0.992 μm^2 6T-SRAM Cell," M. Khare, S.K.H. Fung, R.A. Donaton, S. Greco, C. Brodsky, X. Chen, A. Chou, R. DellaGuardia, S. Deshpande, B. Doris, A. Gabor, M. Gribelyuk, S. Holmes, F. F. Jamin, S.H. Ku, W.L. Lai, W.H. Lee, Y. Li, P. McFarland, S. Mittl, R. Mo, W. Rausch, S. Sankaran, J. Snare, L. Tsou, A. Vayshenker, R. Viswanathan, D. Wehella-Gamag, S. Wu, T. Wagner, W. Yan, E. Barth, R. Ferguson, P. Gilbert, D. Schepis, A. Sekiguchi, R. Goldblatt, J. Welser, K.P. Muller and P. Agnello, presented at *International Electron Devices Meeting*, San Francisco, CA, Dec 2002 (*Technical Digest*, p. 407).
16. "A high-speed, high-sensitivity silicon lateral trench photodetector," M. Yang, K. Rim, D.L. Rogers, J.D. Schaub, J.J. Welser, D.M. Kuchta, D.C. Boyd, F. Rodier, P.A. Rabidoux, J.T. Marsh, A.D. Ticknor, Y. Qingyun, A. Upham, S.C. Ramac, *Electron Device Letters*, **23** (7), Jul 2002, p. 395-7.
17. "Mobility enhancement in strained Si NMOSFETs with HfO_2 gate dielectrics," K. Rim, E.P. Gusev, C. D'Emic, T. Kanarsky, H. Chen, J. Chu, J. Ott, K. Chan, D. Boyd, V. Mazzeo, B.H. Lee, A. Mocuta, J. Welser, S.L. Cohen, M. leong, H.S. Wong, presented at *VLSI Technology Symposium*, Honolulu, HI, June 2002 (*Technical Digest* p. 12-13).
18. "Investigation of silicon nanocrystal floating gate memories," **(Invited)** A. Kumar, J. Welser, S. Tiwari, F. Rana, K. Chan, presented at *Microcrystalline and Nanocrystalline Semiconductors Symposium*, Boston, MA, Nov 2000 (*MRS Proceedings* **638**, 2001, p. 2.4.1-8).
19. "High speed silicon lateral trench detector on SOI substrate," M. Yang, J. Schaub, D. Rogers, M. Ritter, K. Rim, J. Welser, B. Park, presented at *International Electron Devices Meeting*, Washington, DC, Dec 2001 (*Technical Digest* p. 24.1.1-4).
20. "High performance sub 40 nm CMOS devices on SOI for the 70 nm technology node," S. Narasimha, A. Ajmera, H. Park, D. Schepis, N. Zamdmer, K.A. Jenkins, J.O. Plouchart, W.H. Lee, J. Mezzapelle, J. Bruley, B. Doris, J.W. Sleight, S.K. Fung, S.H. Ku, A.C. Mocuta, I. Yang, P.V. Gilbert, K.P. Muller, P. Agnello, J. Welser, presented at *International Electron Devices Meeting*, Washington, DC, Dec 2001 (*Technical Digest* p. 29.2.1-4).

21. "Gate length scaling accelerated to 30 nm regime using ultra thin film PD SOI technology," S.K. Fung, M.H. Khare, D. Schepis, W.H. Woo Lee, S.H. Ku, H. Park, J. Snare, B. Doris, A. Ajmera, K.P. Muller, P. Agnello, P. Gilbert, J. Welser, presented at *International Electron Devices Meeting*, Washington, DC, Dec 2001 (*Technical Digest* p. 29.3.1-4).
22. "A CMOS compatible high speed silicon lateral trench photodetector," M. Yang, K. Rim, D. Rogers, J. Schaub, J. Welser, D. Kuchta, D. Boyd, presented *Device Research Conf.*, Notre Dame, IN, June 2001 (*Tech. Digest* p. 153-4).
23. "Small silicon memories: confinement, single electron, and interface state considerations," S. Tiwari, J.A. Wahl, H. Silva, F. Rana, J. Welser, *Applied Physics A – Materials Science Processing*, **A71** (4), Oct 2000, p. 403-414.
24. "Straddle gate transistor: A MOSFET in the limit of useful field effect," S. Tiwari, A. Kumar, J. Welser, *Int. J. High Speed Electronic Systems*, **10** (1), Mar 2000, p. 231-45. Presented at *DoD Workshop on Future Electronics*, Villard de Lanz, France, June 1999.
25. "A novel trench DRAM cell with a VERTlcal access transistor and BuriEd STRap (VERI BEST) for 4Gb / 16Gb," U. Gruening, C.J. Radens, J.A. Mandelman, A. Michaelis, M. Seitz, N. Arnold, D. Lea, D. Casarotto, A. Knorr, S. Halle, T.H. Ivers, L. Economikos, S. Kudelka, S. Rahn, H. Tews, H. Lee, R. Divakaruni, J.J. Welser, T. Furukawa, T.S. Kanarsky, J. Alsmeier, and G.B. Bronner, presented at *International Electron Device Meeting*, Washington, D.C., Dec 1999 (*Technical Digest* p. 25-28).
26. "Write, erase, and storage times in nano-crystal memories and the role of interface states," J.A. Wahl, H. Silva, A. Gorkirmak, A. Kumar, J.J. Welser, and S. Tiwari, presented at *International Electron Device Meeting*, Washington, D.C., Dec 1999 (*Technical Digest* p. 375-8).
27. "Investigations of silicon nano-crystal floating gate memories," (**Invited**) J.J. Welser, S. Tiwari, F. Rana, A. Kumar, and K. Chan, presented at *CREST Workshop on Silicon Nanofabrication and Nanodevices*, Tokyo, Japan, Sep 1999, (*Digest* p. 15-18).
28. "Straddle gate transistors: High I_{on} / I_{off} transistors at short gate lengths," S. Tiwari, J.J. Welser, A. Kumar, and S. Cohen, presented at *Device Research Conference*, Santa Barbara, CA, June 1999 (*Technical Digest* p. 26-27).
29. "Deep trench capacitor DRAM cell utilizing a vertical transistor sidewall transfer device," J.J. Welser, A. Kumar, T. Furukawa, T.S. Kanarsky, S.J. Holmes, D.V. Horak, N. King, A. Knorr, P.C. Jamison, U. Gruening, C. Radens, J.A. Mandelman, G.B. Bronner, S. Tiwari, and M. Hakey, presented at *Device Research Conference*, Santa Barbara, CA, June 1999 (Late News).
30. "Statistical effects in memories using silicon quantum dots: Transport and interface state issues," S. Tiwari, J.J. Welser, A. Kumar, and F. Rana, presented at *Silicon Nanoelectronics Workshop*, Kyoto, Japan, June 1999.
31. "CMOS and memories: from 100 nm to 10 nm!" S. Tiwari, P.M. Solomon, J.J. Welser, E.C. Jones, F.R. McFeely, and E. Cartier, *Microelectronics Engineering*, **46** (1-4), May 1999, p.3-6. Presented at *International Conference on Micro and Nanofabrication*, Leuven, Belgium, Sep 1998.
32. "Electric-field penetration into metals: Consequences for high-dielectric-constant capacitors," C.T. Black and J.J. Welser, *Transactions on Electron Devices*, **46** (4), Apr 1999, p. 776-780.
33. "Nanoscale CMOS", (**Invited**) H.-S. Philip Wong, D.J. Frank, P.M. Solomon, C.H.J. Wann, and J.J. Welser, *IEEE Proceedings*, **87** (4), Apr 1999, p. 537-570.
34. "Straddle-gate transistor: Changing MOSFET channel length between off- and on-state towards achieving tunneling-defined limit of field-effect," Sandip Tiwari, J.J. Welser, and Paul M. Solomon, presented at *International Electron Devices Meeting*, San Francisco, CA, Dec 1998 (*Technical Digest* p. 737-740).
35. "Role of small dimensions and quantum confinement in small silicon memories," S. Tiwari, F. Rana, A. Kumar, J.J. Welser, and C.T. Black, presented at *Fifth International Symposium on Quantum Confinement: Nanostructures*, Boston, MA, Nov 1998 (*Technical Proceedings* 1999 p. 507-28).
36. "Currents, surface potentials, and defect generation in 1.2 - 1.5 nm oxide MOSFETs," Sandip Tiwari, J.J. Welser, D.J. DiMaria, F. Rana, presented at *Device Research Conference*, Charlottesville, VA, June 1998 (*Technical Digest* p. 12-13).
37. "Kinetic modeling of quantum dots coupled to field-effect transistors," (**Invited**) Farhan Rana, Sandip Tiwari, and J.J. Welser, *Superlattices and Microstructures*, **23** (3-4), Mar/Apr 1998, p.757-770.
38. "Evaluation of the valence band discontinuity of Si/Si_{1-x}Ge_x/Si heterostructures by application of admittance spectroscopy to MOS capacitors," S. Takagi, J.L. Hoyt, K. Rim, J.J. Welser, and J.F. Gibbons, *IEEE Transactions on Electron Devices*, **45** (2), Feb 1998, p.494-501.
39. "Hole mobility improvement in silicon-on-insulator and bulk silicon transistors using local strain," Sandip Tiwari, M.V. Fischetti, P.M. Mooney, and J.J. Welser, presented at *International Electron Devices Meeting*, Washington, D.C., Dec 1997 (*Technical Digest* p. 939-941).

40. "Consequences of confinement effects in the charging and discharging of nano-crystal and quantum-dot memories," (Invited) Sandip Tiwari, Farhan Rana, and J.J. Welser, presented at *International Semiconductor Device Research Symposium*, Charlottesville, VA, Dec 1997.
41. "Technology and power-speed trade-offs in quantum-dot and nano-crystal memory devices," Sandip Tiwari, J. J. Welser, and F. Rana, presented at *VLSI Technology Symposium*, Kyoto, Japan, Jun 1997 (*Proceedings*, p. 133-134).
42. "Room temperature operation of a quantum-dot Flash memory," J.J. Welser, Sandip Tiwari, S. Rishton, K.Y. Lee, and Y. Lee, *Electron Device Letters*, **18** (6), Jun 1997, p. 278-280.
43. "New experimental technique for evaluating band discontinuity -- application of admittance spectroscopy to MOS capacitors fabricated on Si/SiGe/Si heterostructures," S. Takagi, J.L. Hoyt, K. Rim, J.J. Welser, and J.F. Gibbons, presented at *Semiconductor Interface Specialists Conference*, San Diego, CA, Dec 1996.
44. "Importance of inter-valley scattering on the enhancement of phonon-limited mobility in strained-Si MOSFETs," S. Takagi, J.L. Hoyt, J.J. Welser, and J.F. Gibbons, presented at *International Conference on Simulation of Semiconductor Processes and Devices*, Tokyo, Japan, Sep 1996 (*Proceedings*, p. 5-6).
45. "Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal-oxide-semiconductor field-effect transistors," S. Takagi, J.L. Hoyt, J.J. Welser, and J.F. Gibbons, *Journal Applied Physics*, **80** (3), Aug 1996, p.1567-1577.
46. "Resonant cavity photodetectors in silicon-on-insulator," B. Pezeshki, D.M. Kuchta, J.J. Welser, and J.A. Kash, presented at *Conference on Lasers and Electro-Optics*, Anaheim, CA, June 1996.
47. "Wavelength selective waveguide photodetectors in silicon-on-insulator," B. Pezeshki, F. Agahi, J.A. Kash, J.J. Welser, and W.K. Wang, *Applied Physics Letters*, **68** (6), Feb 1996, p. 741-743.
48. "Enhanced hole mobilities in surface-channel strained-Si p-MOSFETs," K. Rim, J. Welser, J.L. Hoyt, and J.F. Gibbons, presented at *International Electron Devices Meeting*, Washington, D.C., Dec 1995 (*Technical Digest*, p.517-520).
49. "Strained-Si MOS field effect transistors: building devices on relaxed Si_{1-x}Ge_x buffer layers,"(Invited) J. Welser, presented at the *Materials' Research Society Spring Meeting*, San Francisco, CA, Apr 1995 (*Strained Layer Epitaxy - Materials, Processing, and Device Applications*, p. 309-320).
50. "Rapid thermal processing based heteroepitaxy: material and device challenges," J.L. Hoyt, P. Kuo, J.J. Welser, R.M. Emerson, and J.F. Gibbons, presented at *Rapid Thermal and Integrated Processing Symposium IV*, San Francisco, CA, Apr 1995 (*Proceedings*, p. 299-310).
51. "Capacitance-voltage characteristics of Si/SiGeC p-MOS capacitors," K. Rim, S. Takagi, J. Welser, J.L. Hoyt, and J.F. Gibbons, presented at the *Materials' Research Society Spring Meeting*, San Francisco, CA, Apr 1995 (*Strained Layer Epitaxy - Materials, Processing, and Device Applications*, p. 327-332).
52. *The Application of Strained-Si / Relaxed-SiGe Heterostructures to MOSFETs*, J.J. Welser, Ph.D. Dissertation, Stanford University, Dec 1994.
53. "Strain dependence of the performance enhancement in strained-Si n-MOSFETs," J. Welser, J.L. Hoyt, S. Takagi, J.F. Gibbons, presented *International Electron Devices Meeting*, San Francisco, CA, Dec 1994 (*Technical Digest*, p. 373-376).
54. "Growth and processing of relaxed Si_{1-x}Ge_x/strained Si structures for MOS applications," J. Welser, J.L. Hoyt, J.F. Gibbons, *Japanese Journal of Applied Physics*, **33**, Part I (4B), Apr 1994, p. 2419-22. Presented at the *International Conference on Solid State Devices as a part of the 5th International Symposium on Silicon Molecular Beam Epitaxy*, Chiba, Japan, Aug 1993 (*SSDM Proceedings*, p. 377-379 & *SiMBE-5 Proceedings*, p. 2419-2422).
55. "Electron mobility enhancement in strained-Si N-type metal-oxide-semiconductor field-effect transistors," J. Welser, J.L. Hoyt, and J.F. Gibbons, *IEEE Electron Device Letters*, **15** (3), Mar 1994, p. 100-102.
56. "Evidence for real-space hot-electron transfer in high mobility, strained-Si multilayer MOSFETs," J. Welser, J.L. Hoyt, and J.F. Gibbons, presented at *International Electron Devices Meeting*, Washington, D.C., Dec 1993 (*Technical Digest*, p. 545-548).
57. "Temperature and scaling behavior of strained-Si N-MOSFETs," J. Welser, J.L. Hoyt, and J.F. Gibbons, presented at *Device Research Conference*, Santa Barbara, CA, June 1993.
58. "NMOS and PMOS transistors fabricated in strained silicon / relaxed silicon-germanium structures," J. Welser, J.L. Hoyt, and J.F. Gibbons, presented at *International Electron Devices Meeting*, San Francisco, CA, Dec 1992 (*Technical Digest*, p. 1000-1002).

INVITED TALKS AND PANELS (SELECTED NON-CONFERENCE PRESENTATIONS)

1. "Nanoelectronics Research," panel presentation at *NSF Nanoscale Science and Engineering Grantee Conference*, Arlington, VA, Dec 2007
2. "NRI Consortium Model," presented at *NSF/SRC Predictive Modeling for Nanomaterials Workshop*, Arlington, VA, Oct 2007.
3. "NRI: Motivation and Challenges," presented at *EE310 Seminar*, Stanford University, Stanford, CA, Jan 2007.
4. "System and Technology Challenges for Nanoscale CMOS," presented at *California NanoSystems Institute*, UCLA, Los Angeles, CA, Nov 2006.
5. "Managing Research in Universities and Industry," presented at *Stanford Social Science and Technology Workshop*, Stanford, CA, Nov 2006.
6. "Design Tools for Nanoscale and Post-CMOS Devices," panel moderator at *NSF/SRC Future Directions for Design Automation Research Forum*, Arlington, VA, Oct 2006.
7. "Challenges for Future Processor and System Design," presented at *EE310 Seminar*, Stanford University, Stanford, CA, Feb 2006.
8. "Technology & Diversity," panel member at *Reaching Out 2005 GLBT MBA Conference*, Boston, MA, Feb 2005.
9. "Enhancing Mobility for High Performance FETs," presented at *IEEE EDS Symposium on Mobility Enhancement for Advanced CMOS Devices*, Sunnyvale, CA, Jun 2005.
10. "Low Power Electronics: Power Challenges in CMOS Technology and Systems," presented at *United States Army Logistics Transformation Agency Telerobotics and Energy Workshop*, Arlington, VA, Aug 2004.
11. "High Performance CMOS Design at IBM," presented at *E4301 Semiconductor Device Physics class*, Columbia University, New York, Apr 2003 & Apr 2004.
12. "High Performance CMOS Device Design," presented at *UCSB, California NanoSystems Institute Seminar*, Feb 2003.
13. "Semiconductor Technology Roadmap: Differentiation Through Innovation," presented at *IBM Design Forum*, Tokyo, Japan and Seoul, South Korea, Oct 2002.
14. "High Performance CMOS Design," presented at MIT, *MTL VLSI Symposium*, Oct 2002.
15. "Recent Advances in CMOS Technology," presented at Columbia Univ., *CISL Seminar Series*, Nov 2001.
16. "High Performance CMOS Design," presented at Cornell University, *Cornell National Nanofabrication Facility (NNF) Colloquia*, Oct 2001.
17. "Investigations of silicon nano-crystal floating gate memories," presented at *CREST Workshop on Silicon Nanofabrication and Nanodevices*, Tokyo, Japan, Sep 1999.
18. "Floating Gate Memories: Flash, Nanocrystal, or Quantum Dot?" presented at *Toshiba Research Laboratory*, Kawasaki, Japan, June 1997.
19. "Quantum dot flash memory," presented at *IBM Si Innovation Seminar*, Dec 1996.
20. "Vertical transistors and nanocrystals: Memory cell structures for gigabit density," presented at *IBM Si Materials Symposium* (hosted by P. Mooney), May 1996.
21. "The application of strained-Si / relaxed-Si_{1-x}Ge_x epitaxy to metal-oxide-semiconductor field-effect transistors," presented at *Electrical and Computer Engineering Department Seminar*, UC-San Diego, May 1995.
22. "The application of strained-Si epitaxy to MOS devices," presented at the *Solid State Electronics Seminar*, Stanford University, Stanford, CA, Jan 1994.
23. "Strained-Si epitaxy and MOS devices," presented Aug 1993:
RCAST, Tokyo University, Tokyo, Japan; NTT LSI Labs, Atsugi, Japan; Hitachi Central Research Labs, Tokyo, Japan; NEC Microelectronics Research Lab, Tskuba, Japan; Sumitomo Electric Research Labs, Yokohama, Japan.