

- TECHNICAL BIOGRAPHY -

Hiroshi Yamada received the B.E. degree in chemistry from Nagoya University, Japan in 1986. He joined the Research & Development Center (forerunner of the Corporate Research & Development Center), Toshiba Corporation, Kanagawa, Japan, in 1986. He is a Senior Research Scientist with the Electron Devices Laboratory, Corporate Research & Development Center, Toshiba Corporation.



Since joining Toshiba Corporation, he has contributed to the development of high-density packaging technology, focusing on the flip-chip interconnection underlying WLCSP (Wafer-Level Chip Scale Packaging) and the high-density 3-D packaging integration technology. In the early of 1990, he was involved in the development of the high I/O pin-count area array solder bump process for flip-chip interconnection by applying the thin-film-metal/polyimide multilayer I/O redistribution process. His accomplishment accelerated innovation of the I/O layout design on the LSI chip from peripheral to area array, leading to the development of WLCSP. Subsequently, he was involved in the development of flip-chip interconnection with underfill resin. The technologies he developed for the flip-chip interconnection have been applied to various semiconductor products.

Moreover, he contributed the development of the 3-D packaging integration to realize a CCD micro-camera visual inspection system integrated in a wireless micromachine device for inspection of inner surface of 10mm ϕ tube in electric power generators. The 3-D packaging integration was developed as part of the Micromachine Project (National Project of Japan) supported by the New Energy and Industrial Technology Development Organization (NEDO) and the Ministry of Economy, Trade and Industry (METI) of Japan. The technology he developed comprises a 3-D sidewall interconnection method involving application of high-aspect-ratio copper sidewall footprint and heterogeneous device (MEMS, LSI) integration involving application of MID interconnection. His achievement led to substantial innovation in the methodology of packaging design for the restricted packaging space micromachine devices.

He received the Best Paper in Session Award for ISHM'97 and IMAPS'99, the Outstanding Paper Award for IMC'96, MES'98, and IMAPS 2000, and the Best Paper Award for JIEP2001, IEEE Transactions on Advanced Packaging Best Paper Award 2003, and Best Paper Award for IEICE 2005. Furthermore, for his outstanding achievement, he received the IEEE Fellow Award "for contributions to packaging technology of integrated circuits" (2007) and the IEICE Electronics Society Award "for pioneering work on wafer-level packaging technology of semiconductor devices" (2008).

He is a member of the Society of Polymer Science, Japan (SPSJ); the Institute of Electronics, Information and Communication Engineers (IEICE); the Institute of Electrical Engineers of Japan (IEEJ); the Japan Institute of Electronics Packaging (JIEP); the International Microelectronics and Packaging Society (IMAPS) and IEEE. He serves on the committees of the following: IEEE VLSI Packaging Workshop in Japan (Program Chair in 2008); IEEE CPMT Society Japan Chapter; Electronic System Packaging Technology, Japan Electronics and Information Technology Industries Association (JEITA); and Research for MEMS Basic Technology of Micromachine Center (nonprofit foundation promoting cooperation among government, academia and industry in Japan).